

COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 Address:

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APPLICATION NO.	FILING DATE	.] • • •	FIRST NAMED INVI	ENTOR		ATTO	RNEY DOCKET NO.
9/314.493	05/18/99	L.IN	•		( <del>c.</del> )	PTLI	N-9801
		MW	42/1007	EXAMINER			
BO-IN LIN					COLLINS.D		
13445 MANDOLI DRIVE				ART U	NIT 11	PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

**Commissioner of Patents and Trademarks** 

10/07/99



# Office Action Summary

Application No.

Applicant(s

CIN

09/3/4,493 Examiner

Deven M. Collins

Group Art Unit 2823



Responsive to communication(s) filed on	·
☐ This action is <b>FINAL</b> .	
Since this application is in condition for allowance except for in accordance with the practice under Ex parte Quayle, 1935	
A shortened statutory period for response to this action is set to is longer, from the mailing date of this communication. Failure to application to become abandoned. (35 U.S.C. § 133). Extension 37 CFR 1.136(a).	o respond within the period for response will cause the
Disposition of Claims  Claim(s)	is/are pending in the application.
Of the above, claim(s)	is/are withdrawn from consideration.
☐ Claim(s)	is/are allowed.
• -	
Claim(s)	is/are objected to.
☐ Claims	are subject to restriction or election requirement.
Application Papers  See the attached Notice of Draftsperson's Patent Drawing  The drawing(s) filed on	ed to by the Examiner.  isapproveddisapproved.  Inder 35 U.S.C. § 119(a)-(d).  the priority documents have been  ber)  International Bureau (PCT Rule 17.2(a)).
Attachment(s)  Notice of References Cited, PTO-892  Information Disclosure Statement(s), PTO-1449, Paper No Interview Summary, PTO-413  Notice of Draftsperson's Patent Drawing Review, PTO-948  Notice of Informal Patent Application, PTO-152	
SEE OFFICE ACTION ON TH	HE FOLLOWING PAGES

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### **DETAILED ACTION**

# Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Mok (5,703,753, dated 12/30/97).

Mok shows the method as claimed in Figures 1-12 with corresponding text. Mok discloses a mounting assembly for a multiple chip module 13 or other circuit module, which includes a printed wiring board 11 having a surface including an array of board contacts 23, a thermally conductive base 15, a first substrate, a second substrate, conductors 21 connecting the interconnect structure 12, a connector between the board and the second substrate, a heat spreader assembly 14, and a fastener which fastens the thermally conductive base 15 to the board and to the heat spreader assembly 14.

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## Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mok (5,703,753, dated 12/30/97) in view of Otsuka (5,949,142, dated 9/7/99) and Inoue (5,909,010, dated 6/1/99).

Mok shows as stated above in 35 U.S.C. 102.

However, Mok does not show a chip size package.

Otsuka discloses a chip size package constituted by a chip 2 on which an integrated circuit is formed, and plated bumps 2a are formed at terminal portions of the integrated circuit, a flexible two-layered printed-circuit board 4 having interlevel conductive bumps 4c for electrically connecting metal patterns 4a formed on the two surfaces of the flexible board, and an anisotropic conductive film 6 for electrically connecting the plated bumps arranged on the chip.

Inoue discloses a CSP (Chip Size Package) including a semiconductor IC chip 5 having input/output terminals 71 along its edges. A small size substrate 1 has a smaller contour than the

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chip and has a plurality of metal terminals 24 arranged along the edges of its bottom, and a plurality of metal bumps 12 arranged on its top in a lattice configuration.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Mok to include a chip size package because of reasonable expectation of achieving the specific result of reducing the production costs without degrading product reliability.

#### Conclusion

- 5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Deven M. Collins whose telephone number is (703) 305-7840. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

**DMC** 

October 1, 1999

Kevin M. Picardat Primary Examiner